

example implementation

space cube (xc3s1000ftg256-4c)

spw_if.vhd

clk	50MHz	DCM generaterd(=locak bus clock)
tx_clk	100MHz	DCM generaterd
rx_clk	166.66MHz	DCM generaterd

spw_timer.vhd

COUNT6US4	320	320*20ns(clk period)=6.4us
COUNT12US8	640	640*20ns(clk period)=12.8us

spw_receiver_sync.vhd

DISCON_COUNT	141	141*6ns(rx_clk period)=850ns
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spw fpga for dio board (xc3s1000ftg256-4c)

spw_if.vhd

clk	100MHz	DCM generaterd(=bus clock & sdram clk & tx_clk)
tx_clk	100MHz	-
rx_clk	166.66MHz	DCM generaterd

spw_timer.vhd

COUNT6US4	640	640*10ns(clk period)=6.4us
COUNT12US8	1280	1280*10ns(clk period)=12.8us

spw_receiver_sync.vhd

DISCON_COUNT	141	141*6ns(rx_clk period)=850ns
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